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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/569,171	02/22/2006	Stephan jo Cecile Henri Theeuwen	NI 031066	7877

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
HO, ANTHONY	
ART UNIT	**PAPER NUMBER**
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/569,171	THEEUWEN ET AL.	
	Examiner	Art Unit	
	Anthony Ho	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 9 is objected to because of the following informalities: A claim cannot depend upon itself. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Van Den Heuvel (US PUB 2002/0102800).

Van Den Heuvel discloses an electronic device and method of manufacturing the same, comprising a LDMOS type transistor provided at a surface of a semiconductor substrate made of silicon, the transistor having a source and a drain that are mutually connected through a channel, which transistor is further provided with a gate electrode and a shield formed as a metal silicide present between the gate and the drain, which drain is provided with a drain extension extending in the substrate towards the channel, the drain having a contact, drain contact and gate being mutually separated through an extension area, characterized in that the shield has a stepped structure in the extension area, and a L-shaped spacer is present between the gate-electrode and shield (Figure 1; entire document).

Claims 1 and 3-11, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Baliga (US Patent 6,545,316).

Baliga discloses an electronic device and method of manufacturing the same, comprising a LDMOS type transistor provided at a surface of a semiconductor substrate made of silicon, the transistor having a source and a drain that are mutually connected through a channel, which transistor is further provided with a gate electrode and a shield formed as a metal silicide present between the gate and the drain, which drain is provided with a drain extension extending in the substrate towards the channel, wherein

the drain extension is provided with a first and a second region, the first region having interfaces with the channel and the second region, the second region having an interface with a contact area within the drain, which first region has a higher dopant concentration than the second region, the ratio of the dopant concentrations in the dirst and second region is in the range of 1.2 to 2.5, the first region and interface between first and second region is substantially present within a shield area defined by a perpendicular projection of the shield on the substrate, the drain having a contact, drain contact and gate being mutually separated through an extension area, characterized in that the shield has a stepped structure in the extension area, the shield is electrically connected to the source through an electrical connection which comprises a capacitor (Figure 9; column 14 – column 15).

Claims 1 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant Admitted Prior Art (AAPA).

AAPA discloses an electronic device and method of manufacturing the same, comprising a LDMOS type transistor provided at a surface of a semiconductor substrate made of silicon, the transistor having a source and a drain that are mutually connected through a channel, which transistor is further provided with a gate electrode between the gate and the drain, which drain is provided with a drain extension extending in the substrate towards the channel, the drain having a contact, drain contact and gate being mutually separated through an extension area, characterized in that the shield has a stepped structure in the extension area (Figure 1; page 3 – page 4).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oh (US Patent 6,448,611) teaches a high power semiconductor device and fabrication method thereof. D'Anna (US Patent 6,063,678) teaches fabrication of lateral RF MOS devices with enhanced RF properties. Williams et al (US Patent 5,514,608) teaches method of making lightly-doped drain DMOS with improved breakdown characteristics. Brech (US Patent 6,870,219) teaches field effect transistor and method of manufacturing same.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Ho whose telephone number is 571-270-1432. The examiner can normally be reached on M-Th: 8:30AM-7:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH
February 24, 2007

JEROME JACKSON
PRIMARY EXAMINER